CLAIMS:

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A semiconductor interconnect structure comprising first level of metal conductor and second level of metal conductor and one level of insulator material formed therebetween, said structure further comprising a dielectric metal contact via formed at said insulator material level for electrically connecting said first metal and second metal conductors, wherein said metal contact via includes metal liner material surrounding said metal contact via, a portion of said metal liner extending partially into an adjacent metal level of said first and second metal levels, in interlocking relation therewith to enhance mechanical strength of said semiconductor interconnect structure.

2. The semiconductor interconnect structure of Claim 1, wherein said adjacent metal level of said first and second metal levels interlocking with said extended portion of said metal liner exhibits increased resistance to electromigration, thereby increasing performance.

3. The semiconductor interconnect structure of Claim 1, forming a back-end-of-line interconnect structure exhibiting improved electromigration resistance.

4. The semiconductor interconnect structure of Claim 1, wherein said one level of insulator material is a low-k dielectric.

5. The semiconductor interconnect structure of Claim 1, further including multiple levels of metal conductors each separated by a level of insulator material formed therebetween, said structure further comprising a metal contact via formed at each said insulator material level for electrically connecting adjacent metal conductor levels, wherein said metal contact via includes metal liner material surrounding said metal

contact via, a portion of said metal liner extending partially into each adjacent metal level of said first and second metal levels, in interlocking relation therewith.

6. The semiconductor interconnect structure of Claim 5, wherein each metal contact via formed at each insulator material level are aligned.

7. The semiconductor interconnect structure of Claim 5, wherein a metal contact via formed at every other insulator material level are aligned and each metal contact via formed at remaining other insulator material levels are offset from an immediate adjacent layer and are aligned.

8. A method of forming a back-end-of-line semiconductor interconnect structure comprising the steps of:

a) forming a first level of metal conductor enclosed in a diffusion barrier material and embedded in a first insulator material layer;

b) forming an insulator cap layer over said first level of metal conductor embedded in said first insulator material layer;

c) forming a second insulator material layer above said insulator cap layer;

d) forming an opening through said second insulator material layer that reaches said first metal conductor level through said formed cap layer to define a contact via opening;

e) forming a diffusion barrier material liner in said etched contact via opening;

f) forming an opening to define a second metal conductor layer, said opening including a portion of said diffusion barrier liner extending partially therein;

g) forming a layer of diffusion barrier liner material in said formed second metal conductor layer opening and in said contact via for lining said second metal conductor level and lining said contact via; and,

h) filling conductive material in said lined contact via opening and in said lined second metal conductor layer for forming said second level of metal conductor layer, wherein said second level of metal conductor layer includes said partially extended portion of diffusion barrier liner material layers of said contact via to enhance mechanical strength of said back-end-of-line semiconductor interconnect structure.

9. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 8, wherein said step g) includes employing a damascene process for forming said layer of diffusion barrier liner material.

10. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 8, wherein said step g) includes employing a dual damascene process for forming said layer of diffusion barrier liner material.

11. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 8, wherein said step f) of forming an opening to define a second metal conductor layer, includes the steps of:

forming one or more planerization layers of material on top said contact via and second insulator material layer;

patterning a region defining a second metal conductor layer region;

etching said one or more planerization layers and a portion of second insulator material in said defined region to a depth 'd' such that a portion of said diffusion barrier liner

material of said contact via remains in said etched region, said etching including opening said contact via.

12. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 11, wherein said step e) of forming a diffusion barrier material liner in said etched contact via opening includes forming diffusion barrier material layer on top said second insulator material layer.

13. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 12, wherein said step of forming one or more planarization layers includes filling said contact via with an organic material and forming an organic material layer on top said deposited diffusion barrier liner material; and, depositing a thin insulator layer thereover.

14. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 13, wherein said etching said one or more planerization layers further includes removing said organic material layer, said formed diffusion barrier material layer and, removing said portion of second insulator material.

15. The method of forming a back-end-of-line semiconductor interconnect structure as claimed in Claim 8, further including the step h) of removing away extra conductive materials and barrier materials by chemical mechanical polishing (CMP).

16. A semiconductor capacitor device comprising a first layer of conductor material forming a bottom node and a first insulator material layer formed thereon; a plurality of metal contact studs formed on said first layer of conductor material having lined sidewall portions extending upwards above a top surface of said insulator material; a second insulator layer formed on said first insulator material layer and conforming to said upward extending lined sidewall portions and, a second layer of conductor material

forming a top node on top said second insulator layer, wherein an area density of said capacitor device is improved.

17. The semiconductor capacitor device as claimed in Claim 16, wherein said second insulator layer comprises a high-k dielectric material.

18. A method of forming a semiconductor capacitor device comprising the steps of:

a) providing a patterned first conductor layer forming a bottom plate of said device;

b) forming a first insulator material layer on top of said patterned first conductor layer;

c) forming a plurality of metal contact studs contacting said first conductor layer and having sidewall liner portions extending upward;

d) recessing said first insulator material layer to a predetermined depth

e) forming a second insulator layer over the plurality of metal contact studs that conforms to extended sidewall liner portions and recesses formed as a result of recessing step d); and,

f) providing a patterned second conductor layer forming a top plate of said device, wherein an area density of said capacitor device is improved.

19. The method of forming a semiconductor capacitor device as claimed in Claim 18, wherein said step c) of forming a plurality of metal contact studs includes forming a plurality of etched via openings, lining said sidewall portions thereof with diffusion barrier materials, and filling said lined via openings with conductor material, said recessing step d) including recessing said first insulator material layer and said filled

material in said lined vias to said predetermined depth to thereby form extended sidewall liner portions.

20. The method of forming a semiconductor capacitor device as claimed in Claim 18, wherein said plurality of metal contact studs comprises an array.

21. A semiconductor heat sink structure comprising: a first layer of heat sink material; a layer of insulator material formed on said first heat sink material layer; a plurality of contact studs extending upwards from said heat sink material layer through said insulator material layer, said contact studs having sidewall portions and filled with heat sink material to improve area density of said heat sink structure.

22. The semiconductor heat sink structure as claimed in Claim 21, wherein said plurality of contact studs comprises an array.

23. The semiconductor heat sink structure as claimed in Claim 21, wherein said layer of insulator material remaining between said formed plurality of contact studs is partially recessed.

24. The method of forming a semiconductor heat sink structure comprising the steps of:

a) providing a patterned heat sink material layer of said structure;

b) forming a first insulator material layer on top of said patterned heat sink material layer;

c) forming a plurality of contact studs contacting said heat sink material layer and having sidewall liner portions extending upward; and,

d) partially recessing said first insulator material layer to a predetermined depth in between said formed contact studs, wherein an area density of said heat sink is increased.

25. The method of forming a semiconductor heat sink structure as claimed in Claim 24, further comprising the step of: filling in the partially recessed openings in said first insulator material layer with material having suitable thermal conductive properties.